CLAIMS

What is claimed is:

1. In an interface circuit of a data storage system, a method for exchanging data with a volatile memory cache circuit, the method comprising the steps of:

providing a command to the volatile memory cache circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit;

moving a data element through the point-to-point channel in accordance with the command; and

receiving status from the volatile memory cache circuit through the point-to-point channel in accordance with the data element.

2. The method of claim 1 wherein the point-to-point channel includes a set of unidirectional links that carries signals from the interface circuit to the volatile memory cache circuit, and wherein the step of providing the command to the volatile memory cache circuit includes the step of:

sending the command to the volatile memory cache circuit through the set of unidirectional links of the point-to-point channel.

3. The method of claim 2 wherein the point-to-point channel further includes another set of unidirectional links that carries signals from the volatile memory cache circuit to the interface circuit, and wherein the step of receiving status from the volatile memory cache circuit includes the step of:

obtaining the status from the volatile memory cache circuit through the other set of unidirectional links of the point-to-point channel.

4. The method of claim 1 wherein the point-to-point channel includes a first set of unidirectional serial links that carries signals from the interface circuit to the volatile memory cache circuit, and a second set of unidirectional serial links that carries signals from the volatile memory cache circuit to the interface circuit; and

wherein the step of moving the data element includes the steps of:

sending the data element to the volatile memory cache circuit through the first set of unidirectional serial links when the command indicates a write transaction; and

obtaining the data element from the volatile memory cache circuit through the second set of unidirectional serial links when the command indicates a read transaction.

5. The method of claim 4 wherein each of the first set of unidirectional serial links and each of the second set of unidirectional serial links is an asynchronous link;

wherein the step of sending includes the step of:

outputting a respective portion of the data element framed with synchronization delimiters to the volatile memory cache circuit through each of the first set of unidirectional serial links when the command indicates a write transaction; and

wherein the step of obtaining includes the step of:

inputting a respective portion of the data element framed with synchronization delimiters from the volatile memory cache circuit through each of the second set of unidirectional serial links when the command indicates a read transaction.

6. The method of claim 4 wherein the step of sending includes the step of:

outputting a respective portion of the data element and a corresponding multiple bit error detection code to the volatile memory cache circuit through each of the first set of unidirectional serial links when the command indicates a write transaction; and

wherein the step of obtaining includes the step of:

inputting a respective portion of the data element and a corresponding multiple bit error detection code from the volatile memory cache circuit through each of the second set of unidirectional serial links when the command indicates a read transaction.

7. The method of claim 4 wherein the step of sending includes the step of:

outputting portions of the data element as data codes through the first set of unidirectional serial links when the command indicates a write transaction;

wherein the step of obtaining includes the step of:

inputting portions of the data element as data codes through the second set of unidirectional serial links when the command indicates a read transaction; and

wherein the data codes belong to an 8B/10B encoding/decoding data space.

8. The method of claim 4, further comprising the step of:

receiving a busy signal from the volatile memory cache circuit through each of the second set of unidirectional serial links after the step of providing the command and before the step of moving the data element.

9. The method of claim 4 wherein the step of providing the command includes the step of:

sending a tag indicator to the volatile memory cache circuit through the first set of unidirectional serial links; and

wherein the step of receiving the status includes the step of:

obtaining a copy of the tag indicator from the volatile memory cache circuit through the second set of unidirectional serial links.

10. The method of claim 1 wherein the step of moving the data element through the point-to-point channel includes the step of:

reading the data element from the volatile memory cache circuit; and

wherein the method further comprises the step of:

processing the read data element within the interface circuit during the step of receiving status from the volatile memory cache circuit.

11. In a volatile memory cache circuit of a data storage system, a method for exchanging data with an interface circuit, the method comprising the steps of:

receiving a command from the interface circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit;

moving a data element through the point-to-point channel in accordance with the command; and

providing status to the interface circuit through the point-to-point channel in accordance with the data element.

12. The method of claim 11 wherein the point-to-point channel includes a set of unidirectional links that carries signals from the interface circuit to the volatile memory cache circuit, and wherein the step of receiving the command from the interface circuit includes the step of:

obtaining the command from the interface circuit through the set of unidirectional links of the point-to-point channel.

13. The method of claim 12 wherein the point-to-point channel further includes another set of unidirectional links that carries signals from the volatile memory cache circuit to the interface circuit, and wherein the step of providing status to the interface circuit includes the step of:

sending the status to the interface circuit through the other set of unidirectional links of the point-to-point channel.

14. The method of claim 11 wherein the point-to-point channel includes a first set of unidirectional serial links that carries signals from the interface circuit to the volatile memory cache circuit, and a second set of unidirectional serial links that carries signals from the volatile memory cache circuit to the interface circuit; and wherein the step of moving the data element includes the steps of:

obtaining the data element from the interface circuit through the first set of unidirectional serial links when the command indicates a write transaction; and

sending the data element to the interface circuit through the second set of unidirectional serial links when the command indicates a read transaction.

15. The method of claim 14 wherein each of the first set of unidirectional serial links and each of the second set of unidirectional serial links is an asynchronous link;

wherein the step of obtaining includes the step of:

inputting a respective portion of the data element framed with synchronization delimiters from the interface circuit through each of the first set of unidirectional serial links when the command indicates a write transaction; and

wherein the step of sending includes the step of:

outputting a respective portion of the data element framed with synchronization delimiters to the interface circuit through each of the second set of unidirectional serial links when the command indicates a read transaction.

16. The method of claim 14 wherein the step of obtaining includes the step of:

inputting a respective portion of the data element and a corresponding multiple bit error detection code from the interface circuit through each of the first set of unidirectional serial links when the command indicates a write transaction; and

wherein the step of sending includes the step of:

outputting a respective portion of the data element and a corresponding multiple bit error detection code to the interface circuit through each of the second set of unidirectional serial links when the command indicates a read transaction.

17. The method of claim 14 wherein the step of obtaining includes the step of:

inputting portions of the data element as data codes through the first set of unidirectional serial links when the command indicates a write transaction;

wherein the step of sending includes the step of:

outputting portions of the data element as data codes through the second set of unidirectional serial links when the command indicates a read transaction; and

wherein the data codes belong to an 8B/10B encoding/decoding data space.

18. The method of claim 14, further comprising the step of:

sending a busy signal to the interface circuit through each of the second set of unidirectional serial links after the step of receiving the command and before the step of moving the data element.

19. The method of claim 14 wherein the step of receiving the command includes the step of:

obtaining a tag indicator from the interface circuit through the first set of unidirectional serial links; and

wherein the step of providing status includes the step of:

sending a copy of the tag indicator to the interface circuit through the second set of unidirectional serial links.

20. The method of claim 11 wherein the step of moving the data element through the point-to-point channel includes the step of:

providing the data element to the interface circuit; and

wherein the step of providing the status message includes the step of:

sending the status message to the interface circuit such that the status includes (i) a non-reserved value as a tag indicator when the data element is valid, and (ii) a reserved value as the tag indicator when the data is invalid.

21. A data storage system, comprising:

a volatile memory cache circuit that buffers data elements exchanged between a storage device and a host;

an interface circuit that operates as an interface between the volatile memory cache circuit and at least one of the storage device and the host; and

a point-to-point channel, interconnected between the volatile memory cache circuit to the interface circuit, that carries the data elements between the volatile memory cache circuit and the interface circuit.

22. The data storage system of claim 21 wherein the point-to-point channel includes a set of unidirectional links that is capable of carrying a command from the interface circuit to the volatile memory cache circuit.

23. The data storage system of claim 22 wherein the point-to-point channel further includes another set of unidirectional links that is capable of carrying status from the volatile memory cache circuit to the interface circuit.

24. The data storage system of claim 21 wherein the point-to-point channel includes a first set of unidirectional serial links that carries signals from the interface circuit to the volatile memory cache circuit, and a second set of unidirectional serial links that carries signals from the volatile memory cache circuit to the interface circuit.

25. The data storage system of claim 24 wherein each of the first set of unidirectional serial links and each of the second set of unidirectional serial links is an asynchronous link; wherein the interface circuit is configured to provide a respective portion of a data element framed with synchronization delimiters to the volatile memory cache circuit through each of the first set of unidirectional serial links during a write transaction; and wherein the interface circuit is configured to obtain a respective portion of a data element framed with synchronization delimiters from the volatile memory cache circuit through each of the second set of unidirectional serial links during a read transaction.

26. The data storage system of claim 24 wherein the interface circuit is configured to provide a respective portion of a data element and a corresponding multiple bit error detection code to the volatile memory cache circuit through each of the first set of unidirectional serial links during a write transaction; and wherein the interface circuit is configured to obtain a respective portion of a data element and a corresponding multiple bit error detection code from the volatile memory cache circuit through each of the second set of unidirectional serial links during a read transaction.

27. The data storage system of claim 26 wherein the interface circuit is configured to provide portions of a data element as data codes to the volatile memory cache circuit through the first set of unidirectional serial links during a write transaction; and wherein the interface circuit is configured to obtain portions of a data element as data codes from the volatile memory cache circuit through the second set of unidirectional serial links during a read transaction; and wherein the data codes belong to an 8B/10B encoding/decoding data space.

28. The data storage system of claim 24 wherein the volatile memory cache circuit is configured to provide a busy signal to the interface circuit through each of the second set of unidirectional serial links after receiving a command and before a data element moves through the point-to-point channel.

29. The data storage system of claim 24 wherein the interface circuit is configured to provide a tag indicator to the volatile memory cache circuit through the first set of unidirectional serial links when providing a command to the volatile memory cache circuit; and wherein the volatile memory cache circuit is configured to provide a copy of the tag indicator to the interface circuit through the second set of unidirectional serial links when providing status to the interface circuit.

30. An interface circuit for a data storage system, comprising:

a first adaptor that couples to at least one of a storage device and a host;

a second adaptor that couples to a point-to-point channel leading to a volatile memory cache circuit which is capable of buffering data elements exchanged between the storage device and the host; and

a controller, coupled to the first adaptor and the second adaptor, that is configured to:

provide a command to the volatile memory cache circuit through the point-to-point channel;

move a data element between the interface circuit and the volatile memory cache circuit, through the point-to-point channel in accordance with the command; and

receive a status message from the volatile memory cache circuit through the point-to-point channel in accordance with the data element.

31. A volatile memory cache circuit for a data storage system, comprising:

an adaptor that couples to a point-to-point channel leading to an interface circuit which operates as an interface between the volatile memory cache circuit and at least one of a storage device and a host;

memory locations that are capable of buffering data elements exchanged between the storage device and the host; and

a controller, coupled to the adaptor and the memory locations, that is configured to:

receive a command from the interface circuit through the point-to-point channel;

move a data element between the volatile memory cache circuit and the interface circuit, through the point-to-point channel in accordance with the command; and

provide a status message to the interface circuit through the point-to-point channel in accordance with the data element.